Remarks

This Response is considered fully responsive to the Office Action mailed June 11, 2007. Claims 1-23 were pending in the application. Claims 1-23 stand rejected. In this Response, no claims have been amended, added, or cancelled. Claims 1-23 are now pending in the application. Reexamination and reconsideration are requested.

Allowable Subject Matter

Claim 4 has been indicated as allowable.

Rejections Under 35 U.S.C. § 103

Claims 1 and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 7,007,201 to Byrne, et al. ("Byrne") in view of U.S. Patent No. 6,886,057 to Brewer, et al. ("Brewer"). All rejections are respectfully traversed.

The Office alleges that it would have been obvious to a person skilled in the art at the time the invention was made to have included the differential serial channel as taught by Brewer in the invention of Byrne because "use of a differential serial bus as taught by Brewer improves system performance while using a minimal amount of resources." Office Action at page 5. Applicant respectfully submits, however, that neither Byrne nor Brewer expressly or impliedly suggests the asserted combination, as recited in independent claim 1. Indeed, Applicant notes no such contention in the Office Action. Thus, as part its initial burden to establish a *prima facie* case of obviousness, the Office "must present a convincing line of reasoning as to why the artisan would have found the claimed invention to be obvious in light of the teachings of the references. MPEP §2142, citing *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985).

Section 2142 of the Manual of Patent Examining Procedure ("MPEP") explains that a *prima facie* case of obviousness requires that there be some suggestion or motivation, either in the references themselves of in the knowledge of one of ordinary skill in the art, to modify or combine reference teachings. It is for this reason that the mere fact that a combination can be made is legally insufficient to support an obviousness rejection. MPEP §2143.01. The Office bears the initial burden of factually supporting any *prima facie* conclusion of obviousness.

If the Office does not produce a *prima facie* case, the Applicant is under no obligation to submit evidence of nonobviousness. MPEP §2142. Applicant respectfully submits that such is the case in the present application.

At page 5 of the Office Action, the Office alleges that one of ordinary skill in the art would have been motivated to modify Byrne in view of Brewer "improve[s] system performance while using a minimal amount of resources." This line of reasoning, however, does not meet the MPEP's required standard of "convincing" because Byrne teaches that "[t]he signal TRACE_PORT may provide a **real time trace capability** for the selected processor 12 **without disrupting the software being executed.**" Byrne at col. 3, lines 37-39 (Emphasis added). Thus, according to Byrne, real time trace capability is provided without interfering with software execution. As real time trace capability is provided Byrne, there is no need to make the asserted modification to improve system performance over the existing real time trace capability. Consequently, the Office Action fails to provide the required "convincing line of reasoning" required by the MPEP.

The absence of this convincing line of reasoning and any other suggestion for the asserted combination precludes a *prima facie* case of obviousness. For at least this reason, and those set forth above, the rejection of independent claim 1, and those claims depending directly or indirectly therefrom, under 35 U.S.C. § 103 are respectfully traversed. *See* MPEP §2142.

Accordingly, independent claim 1 and those claims depending directly or indirectly therefrom are believed to patentably distinguish over the cited art. Reconsideration and allowance of claim 1, and those claims depending therefrom, are respectfully requested.

Claims 2, 5, 6, and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Byrne in view of Brewer and further in view of NS (*SCAN921023 and SCAN921224 20-66 Mhz 10 Bit Bus LVDS*). Claims 9-11, 13-17, and 19-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Byrne in view of NS. All rejections are respectfully traversed.

Applicant respectfully the Office has also failed to present a convincing line of reasoning for the asserted combination of NS with Byrne and/or Brewer, as the fact that the NS reference can be combined with Byrne and/pr Brewer is legally insufficient to establish a *prima facie* case of obviousness. The Office has provided no motivation for combining NS with Byrne and Brewer. Rather, the Office has merely stated that it would be obvious to combine the references, and that "the use of a differential transmitter as taught by NS increases the speed at which serial

data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering problems." While the combination of NS with Byrne may result in an increase of the speed at which serial data is transmitted from a testing device to an analyzer, this conclusory statement does not articulate any reasoning as to why one of ordinary skill in the art would have combined Byrne, which relates to a shared embedded trace macrocell with the serializer/deserializer taught by NS.

The Office cites NS at paragraph 1, which states that a parallel bus is replaced with a high-speed serial bus. The Office alleges that "[t]his replacement inherently allows for faster transmission of data, which in turn allows for a faster capability for debugging." Office Action at page 3. However, Byrne explicitly states that "[t]he Embedded Trace Macrocell (ETM) [] allows for **real time debug via an external trace port**. The ETM has triggering facilities and a FIFO that allow for transfer of both instructions and data through the trace port to an external trace port analyzer hardware without stalling the microprocessor." Byrne at col. 1, lines 16-21. Thus, Byrne already allows for real time debugging, without the additional teachings of NS. No motivation exists to combine NS with Byrne because debugging cannot occur faster than real time.

Further, Applicant respectfully submits that the motivation articulated by the Office is based on impermissible hindsight. *See* MPEP §2143.01. An obviousness determination may "take[s] into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned only from applicant's disclosure." *In re McLaughlin*, 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971). In the instant case, the motivation proposed by the Office for combining Byrne with NS appears to be **gleaned directly from Applicant's Specification** and, thus, is impermissible. Specifically, paragraph [0007] of the present pending application states "It would thus be desirable to provide a system and method for providing a debugging environment that uses a high speed serial interface to provide a debug interface between an IC device being debugged and a control console/workstation such that the IC device can run at its normal, high speed, thereby enabling real time emulation of an SOC device having a serial debug port." As the cited references fail to discuss any debug interface between an IC device being debugged and a control console/workstation, no motivation exists to "increase the speed at which data is transmitted from a testing device to an analyzer."

For at least these reasons, and those set forth above, the rejections of claims 2, 5, 6, 8-11, 13-17, and 19-23 under 35 U.S.C. §103 are respectfully traversed. Reconsideration and allowance of the claims are respectfully requested.

Claims 7, 12, and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Byrne in view of NS, and further in view of U.S. Publication No. 2006/0288254 by Agarwala, et al., ("Agarwala"). All rejections are respectfully traversed.

Applicant respectfully submits that Agarwala fails to cure the deficiencies of Byrne and NS discussed above. Thus, Claim 7 is believed to patentably distinguish over the cited art for at least the same reasons as those claims from which it depends. Reconsideration and withdrawal of the rejection of claim 7 is respectfully requested.

Further, Applicant respectfully submits that there is no "convincing line of reasoning" presented as to the Office's rationale for combining the teachings of Agarwala with Byrne and/or NS, and that the motivation provided by the Office is a product of impermissible hindsight for at least the same reasons as discussed with respect to Byrne and NS. Specifically, as Byrne teaches debugging in real time, no need exists to transmit data more quickly, or to conserve communication bandwidth. Additionally, the product of Byrne and NS provides for "faster transmission of data" without the modifications taught by Agarwala. Regarding the Office's assertion that combining Agarwala with Byrne and NS would have been obvious because it allows for "conservation of inter/extra-circuit communication bandwidth," Applicant respectfully submits that this alleged motivation is also the product of impermissible hindsight. In the instant case, the motivation proposed by the Office for combining Agarwala with Byrne and NS also appears to be **gleaned directly from Applicant's Specification**. Specifically, the present pending application at paragraph [0031] states "In an alternate embodiment to the present invention, a lossless compression technique such as Huffman or LZW coding is provided to further reduce data transmission bandwidth requirements by reducing the overall amount of data required to be transmitted to the debugging tool 106 (shown in FIG. 1)." As the cited references fail to discuss any debug interface between an IC device being debugged and a control console/workstation or transmission of trace data, no motivation exists to conserve "inter/extra-circuit communication bandwidth."

For at least these reasons, Applicant respectfully submits that the Office has failed to establish a *prima facie* case of obviousness, and claims 7, 12, and 18 patentably distinguish over the cited art. Reconsideration and allowance of claims 7, 12, and 18 are respectfully requested.

Conclusion

Claims 1-23 are currently pending in the application. Applicant has fully responded to each and every objection and rejection in the Office action dated January 8, 2007 and believes that claims 1-23 are in a condition for allowance. Applicant therefore requests that a timely Notice of Allowance be issued in this case.

A petition for a three month extension of time is submitted herewith. The Applicant believes no other fees or petitions are due with this filing. However, should any such fees or petitions be required, please consider this a request therefor and authorization to charge Deposit Account No. 50-3199 as necessary.

If the Examiner should require any additional information or amendment, please contact the undersigned attorney. If the Examiner believes any issues could be resolved via a telephone interview, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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